GLOBALFOUNDRIES Solidifies 14nm FinFET Design Infrastructure for Next-Generation Chip Designs

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In collaboration with design ecosystem partners, GLOBALFOUNDRIES provides digital design flows for customers designing on leading-edge technology

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- In partnership with leading EDA providers Cadence, Mentor Graphics, and Synopsys, GF develops new digital design flows.
- New digital design starter kit integrates process design kit (PDK) and early access standard cell libraries.
- The new design flows have been optimized to solve challenges associated with the critical design rules of 14nm FinFET technology.

GF, a leading provider of advanced semiconductor manufacturing technology, today announced it has reached a critical milestone in providing a robust design infrastructure for its 14-nanometer (nm) FinFET process technology, supporting customer's design starts on the foundry's latest manufacturing technology node.

Together with key ecosystem partners Cadence Design Systems, Mentor Graphics, and Synopsys, GF has developed new digital design flows for register-transfer level (RTL) to graphic design database system (GDS) implementation. Integrated with a technology-proven process design kit (PDK) and early-access standard cell libraries, the flows create a digital design "starter kit" that provides designers with a built-in test case for out-of-the-box physical implementation testing and analysis of performance, power and area.

"GF is committed to providing our customers with advanced technology platforms that include the comprehensive design infrastructure required to optimize design productivity and cycle time," said Rick Mahoney, senior vice president of design enablement at GF. "To ensure our design ecosystem delivers the highest quality experience with our 14nm FinFET technology, GF has collaborated with our EDA partners to complement our in-house global design capabilities and accelerate time-to-volume of designs on complex technologies like 14nm FinFET."

GF's digital design flows have been optimized to solve the challenges associated with the critical design rules of the 14nm technology node and includes newly introduced features such as implant-aware placement and double-patterning aware routing, In-Design DRC™ fixing and yield improvement, local/random variability aware timing, 3D FinFET extraction, and color-aware LVS/DRC sign-off.

The Synopsys-based Design Enablement Starter Kit leverages broad capabilities of its Galaxy™ Design Platform to deliver signed-off GF's 14LPP FinFET designs with optimized performance, power and area. Synopsys' Design Compiler® Graphical synthesis, coupled with its Formality® equivalence checking solution, streamlines the flow by providing physical guidance and results that closely correlate with physical implementation. For FinFET implementation, Synopsys' IC Compiler™, IC Compiler II and IC Validator solutions provide implant- and double-patterning-aware placement and routing with In-Design color-aware physical verification. Synopsys' StarRC™ extraction provides double-patterning support, with modeling for color-aware and 3-D extraction essential for 14nm designs. In addition, the industry-standard Synopsys PrimeTime® sign-off solution for accurate delay calculation, timing analysis and advanced waveform propagation accurately accounts for FinFET impacts such as ultra-low voltage, increased Miller effect and resistivity, and process variation.

To enable customers to achieve the benefits of GF's 14LPP node at the design level, GF and Cadence have worked together to create a digital flow for a complete RTL-to-GDSII FinFET solution. The digital flow integrates and optimizes Cadence's front-end, back-end, physical verification, and DFM solutions for 14LPP technology. For front-end design, Cadence's RTL Compiler synthesis flow is fine-tuned with the 14LPP library. For physical implementation, both Encounter® Digital Implementation System (EDI) and Innovus™ Implementation System provide color-aware double-patterning technology for correct-by-construction placement and routing, and customized settings for the 14LPP design rules and library to optimize power, performance and area (PPA). In-design PVS DRC fixing and in-design litho hot-spot fixing are both available to designers to reduce design iterations and ease design closure. For signoff, the flow features fully integrated Quantus QRC Parasitic Extraction and Tempus Timing Signoff solutions. Integration within both EDI and Innovus allows Quantus and Tempus to bring advanced process modeling earlier in the P&R flow for better timing convergence and time-to-tapeout. Encounter Conformal® Equivalence Checker is embedded in multiple stages in the implementation flow. Voltus power and EMIR analysis, standalone Physical Verification System physical verification and Litho Physical Analyzer litho hot-spot check are also embedded in the reference flow. The reference flow provides a guided approach to Cadence's tool suite and the GF 14LPP process to ensure designers hit the maximum PPA envelope with minimum ramp-up time.

As with production tape-outs at prior nodes, the starter kit uses the Mentor Graphics Calibre® tool suite for sign-off. In the case of

the 14nm starter kit, the Calibre nmDRC™ and Calibre MultiPatterning products are used for layer decomposition, DRC verification and metal filling, while the Calibre nmLVS™ product is used for logic verification.

GF 14nm FinFET technology is among the most advanced in the industry, offering an ideal solution for the most demanding high-volume, high-performance and power-efficient SoC designs. The 3D FinFET devices offers the perfect answer to growing market needs, with best-in-class intrinsic performance boost over 28nm technology and a superior power footprint compared to any predecessors. These leading edge devices also provide a true cost advantage due to superior power, performance and area scaling.

GF is yielding on its 14nm technology and is on schedule to support multiple product tape-outs and volume ramp in 2015.

Through GF's design partnership ecosystem, designers have access to a broad spectrum of services such as system design, embedded software design, SoC design and verification, and physical implementation. These include design flows for electronic design automation (EDA); silicon-proven IP building blocks, such as libraries; and simulation and verification design kits, i.e., process design kits (PDK) and technology files.

ABOUT GF

GF is the world’s first full-service semiconductor foundry with a truly global footprint. Launched in March 2009, the company has quickly achieved scale as the second largest foundry in the world, providing a unique combination of advanced technology and manufacturing to more than 160 customers. With operations in Singapore, Germany and the United States, GF is the only foundry that offers the flexibility and security of manufacturing centers spanning three continents. The company’s three 300mm fabs and five 200mm fabs provide the full range of process technologies from mainstream to the leading edge. This global manufacturing footprint is supported by major facilities for research, development and design enablement located near hubs of semiconductor activity in the United States, Europe and Asia. GF is owned by Mubadala Development Company. For more information, visit http://www.globalfoundries.com.

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