Cadence and GLOBALFOUNDRIES Announce First Test Chip Featuring ARM Cortex-A12 Processor in 28nm-SLP Process

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Highlights:

- Test chip designed to demonstrate performance and power characteristics of ARM® Cortex®-A12 processor on GLOBALFOUNDRIES 28nm-SLP process
- Achieved maximum frequency of 2.0GHz in 15 weeks using the full Cadence RTL-to-GDSII digital implementation and signoff solutions
- Full suite of Cadence signoff tools used, including QRC Extraction, Tempus Timing Signoff Solution and the Physical Verification System

SAN JOSE, Calif., March 12, 2014—At CDNLive Silicon Valley 2014, Cadence Design Systems Inc. and GF announced that they have taped out a quad core test chip built around the ARM Cortex-A12 processor. Targeted to operate at frequencies of up to 2.0GHz while still within the mainstream mobile power and area envelope, the test chip is implemented in GF's 28nm-SLP (Super Low Power 28 nanometer High-K Metal Gate) process using a full Cadence® tool flow and incorporates ARM POP™ technology to leverage the full performance range of the 28-SLP process.

The Cortex-A12 processor provides a 40 percent performance increase and direct upgrade path from ARM's highly successful Cortex-A9 processor, while matching the energy efficiency of its predecessor. The successful tapeout marks an important move toward the incorporation of the Cortex-A12 core in mobile applications such as smartphones and tablets.

"As the lead foundry working with the Cortex-A12 processor, we collaborated closely with Cadence and ARM to implement this new core using our 28nm low-power process, and ARM libraries specifically tuned to meet demanding mobile market requirements," said Ana Hunter, vice president of product management at GF. "This test chip will be instrumental in showing our mutual customers how they can productize and reap the benefits from the Cortex-A12 processor in conjunction with the 28nm-SLP process using a Cadence flow."

"The ARM Cortex-A12 processor is a high-performance compute solution that will benefit developers looking to upgrade existing mid-range mobile products as well as expanding our technology into a new range of electronic devices such as set-top boxes," said Dipesh Patel, executive vice president and general manager, physical design group, ARM. "The work by ARM, Cadence and GF in jointly developing a test chip on 28nm utilizing ARM POP IP will accelerate its time to market."

The full Cadence RTL-to-signoff digital implementation flow was used, including Encounter® RTL Compiler, Encounter RTL Compiler with Physical, Encounter Digital Implementation System and Encounter Conformal Equivalence Checker. The full suite of Cadence signoff tools were also used, including QRC Extraction, Tempus™ Timing Signoff Solution and the Physical Verification System, closing final signoff and achieving tapeout in 15 weeks from RTL availability.

"Projects like this Cortex-A12 processor test chip are important milestones, and can only be achieved through tight collaboration," said Anirudh Devgan, senior vice president of the Digital and Signoff Group at Cadence. "Our work with GF and ARM will be welcome news for electronics companies interested in exploring ARM's newest core."

GF's 28nm-SLP technology is ideally suited for the next generation of smart mobile devices, enabling designs with faster processing speeds, smaller feature sizes, lower standby power and longer battery life. The technology is based on GF's "Gate First" approach to High-K Metal Gate (HKMG), which has been in volume production for nearly three years. The technology offers a combination of performance, power efficiency and cost that is ideally suited for the mobile market.

POP technology contains ARM Artisan® Physical IP logic libraries and memory instances specifically tuned for a given ARM core and process technology, a comprehensive benchmarking report to pinpoint exact conditions and results ARM achieved for core implementation, and POP implementation knowledge including a user guide, floor plans and scripts. POP IP products are currently available from 40nm to 28nm, with a roadmap down to 14nm process technology for a wide range of Cortex-A processor series CPU and Mali™ GPU products.

GF will deliver a presentation on their joint work at CDNLive Silicon Valley on March 12. The presentation is titled, "A Power-, Performance-, and Cost-Optimized Cortex-A12 Implementation in 28nm-SLP (Super-Low-Power) Technology"

About Cadence

Cadence enables global electronic design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use Cadence software, hardware, IP, and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. The company is headquartered in

San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry. More information about the company, its products, and services is available at www.cadence.com.

About GF

GF is the world's first full-service semiconductor foundry with a truly global footprint. Launched in March 2009, the company has quickly achieved scale as the second largest foundry in the world, providing a unique combination of advanced technology and manufacturing to more than 160 customers. With operations in Singapore, Germany and the United States, GF is the only foundry that offers the flexibility and security of manufacturing centers spanning three continents. The company's three 300mm fabs and five 200mm fabs provide the full range of process technologies from mainstream to the leading edge. This global manufacturing footprint is supported by major facilities for research, development and design enablement located near hubs of semiconductor activity in the United States, Europe and Asia. GF is owned by the Advanced Technology Investment Company (ATIC). For more information, visit http://www.globalfoundries.com.

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