GLOBALFOUNDRIES Accelerates Adoption of 20nm-LPM and 14nm-XM FinFET Processes with Comprehensive Production-Ready Design Flows

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Jointly developed with leading EDA providers, flows address AMS challenges from specification to verification; complete flows for digital design for double patterning

Milpitas, Calif. — May 30, 2013 –At next week's 50th Design Automation Conference (DAC) in Austin, Texas, GLOBALFOUNDRIES will unveil a comprehensive set of certified design flows to support its most advanced manufacturing processes. The flows, jointly developed with the leading EDA providers, offer robust support for implementing designs in the company's 20nm low power process and its leading-edge 14nm-XM FinFET process. Working closely with Cadence Design Systems, Mentor Graphics and Synopsys, GF has developed the flows to address the most pressing design challenges, including support for analog/mixed signal (AMS) design, and advanced digital designs, both with demonstration of the impact of double patterning on the flow.

The GF design flows work with its process design kits (PDKs) to provide real examples that demonstrate the entire flow. The user can download the design database, the PDK, detailed documentation and multi-vendor scripts to learn how to set up and use the GF design flow. The flows use open source examples and provide the customer with working, executable and customizable flows.

"As the developer of the industry's first modular 14nm FinFET technology and one of the leaders at 20nm, we understand that enabling designs at these advanced process nodes requires innovative methodologies to address unprecedented challenges," said Andy Brotman, vice president of design infrastructure at GF. "By working with a new level of collaboration with EDA partners, we can provide enhanced insight into our manufacturing processes in order to fully leverage the capabilities of 20nm and 14nm manufacturing. This provides our mutual customers with the most efficient, productive and risk-reduced approach to achieving working silicon."

Production Ready AMS flow from specification to verification

To address the unique requirements of analog/mixed signal (AMS) design at advanced processes, GF has enhanced its design flows to provide production quality scripts and packaged methodologies. The new reference flow establishes a working flow from specification to physical verification that has been taped out to be verified on working silicon.

The AMS reference flow provides comprehensive double pattern design guidelines. It gives overview of decomposition flow for both block level and chip level. The flow also addresses decomposition for different design styles. Recommendations for color balancing, hierarchical decomposition, ECO changes are discussed. The flows also present decomposition impact on DRC run time and resulted database size.

Notably, the reference flow includes support for efficiency and productivity improvements in the Cadence Virtuoso® environment specifically for designing in a double patterned process. The flow includes support for Virtuoso Advanced Node 12.1 and provides efficient access to the tool's productivity benefits for physical design with real-time, color-aware layout. Circuit designers can assign "same net" constraints in the schematic, and the layout designers can meet these requirements as they create the physical view. Additionally, layout designers can take advantage of Virtuoso tool support for local interconnect, and advanced layout dependent effect management.

The flow also features interoperability with Mentor's Calibre® nmDRC™, nmLVS™, and extraction products which address multipatterning requirements for both double and triple patterning. In addition special settings for analog design; auto-stitching and when to use it; and fill and color balancing are described in detail.

The AMS flow provides detailed information on parasitic extraction and layout dependent effects, both of which introduce new challenges at 20nm and 14nm. For parasitic extraction, the flows are described in detail and customizable scripts and examples demonstrate OA and DSPF back annotation. In addition the flows illustrate methodologies to predict layout-dependent effects during schematic design and methods to include full models in post layout extraction. PEX flows for Synopsys StarRC™ extraction, Cadence QRC and Mentor CalibrexRC™ are supported.

These flows serve as references to validate the correctness of the accompanying PDK as well as the vendor tools setup.

Sign-off ready RTL2GDSII flows that address double patterning

GF is also making available new flows that support a complete RTL-to-GDSII design methodology for targeting its 20nm and 14nm manufacturing processes. The company worked with EDA vendors to certify the flows in their respective environments and provide a platform for optimized, technology-aware methodologies that take full advantage of the performance, power and area benefits of the processes.

The result is a set of fully executable flows containing all the scripts and template files required to develop an efficient methodology. The flows serve as a reference to validate the correctness of the accompanying PDK as well as the vendor tool setup. In addition the flows offer access to other critical and useful information, such as methodology tutorial papers; guidelines and methodologies for decomposition of double patterned layouts; PEX/STA methodology recommendations and scripts; and design guidelines and margin recommendations.

A critical aspect of manufacturing at this level is the use of double patterning, an increasingly necessary technique in the lithographic process at advanced nodes. Double patterning extends the ability to use current optical lithography systems and the GF flows provide comprehensive double pattern design guidelines. They address design for double patterning and the added flow steps for different design styles and scenarios.

This includes support for odd cycle checking, a new type of DRC rule that must be met to allow for legal decomposition of the metals into two colors. This check is detailed in the flow and guidelines are provided to make sure it is met.

Synopsys and GF worked together to minimize the impact of changes associated with the 3-D nature of FinFET devices as compared to planar transistors. The two companies focused on making FinFET adoption transparent to the design team. The collaboration on Synopsys' RTL to GDSII flow includes 3-D parasitic extraction with the Synopsys StarRC™ tool, SPICE modeling with the Synopsys HSPICE® product, routing rules development with the Synopsys IC Compiler™ tool and static timing analysis with the Synopsys PrimeTime® tool.

Cadence contributed a complete RTL-GDSII flow, including physical synthesis, and planning and routing developed with the Encounter® Digital Implementation (EDI) System foundation flow. The seamless implementation flow, using Cadence Encounter RTL Compiler and EDI System, supports double patterning and advanced 20- and 14-nm routing rules.

Mentor's Olympus-SoC™ place and route system is supported in the flow, providing support for new DRC, double patterning, and DFM rules. The Olympus-SoC router has its own native coloring engine along with verification and conflict resolution engines that detect and automatically fix double patterning violations. Expanded features include DP-aware pattern matching, coloring aware pin access, pre-coloring of critical nets, and DP aware placement. The Calibre® InRoute™ product allows Olympus-SoC customers to natively invoke Calibre signoff engines during design for efficient and faster manufacturing closure.

Double patterning also impacts LVS and other DRC issues, and the flows provide methodology details to address these areas, including hierarchical decomposition to reduce data base explosion. Parasitic extraction methodologies and scripts are provided as well, offering ways to address double patterning-induced variations via DPT corners or with maskshift PEX features.

About GF

GF is the world's first full-service semiconductor foundry with a truly global footprint. Launched in March 2009, the company has quickly achieved scale as the second largest foundry in the world, providing a unique combination of advanced technology and manufacturing to more than 160 customers. With operations in Singapore, Germany and the United States, GF is the only foundry that offers the flexibility and security of manufacturing centers spanning three continents. The company's three 300mm fabs and five 200mm fabs provide the full range of process technologies from mainstream to the leading edge. This global manufacturing footprint is supported by major facilities for research, development and design enablement located near hubs of semiconductor activity in the United States, Europe and Asia. GF is owned by the Advanced Technology Investment Company (ATIC). For more information, visit http://www.globalfoundries.com.