GLOBALFOUNDRIES Introduces Certified Design Flows for Multi-Die Integration Using 2.5D IC technology

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Collaboration with leading EDA vendors supports complete range of steps required to create and verify advanced stacking implementations using TSV and interposer approaches

Milpitas, Calif. — May 30, 2013 –At next week's 50th Design Automation Conference (DAC) in Austin, Texas,GLOBALFOUNDRIES will unveil a comprehensive set of certified design flows to support 2.5D IC product development with its most advanced manufacturing processes. The sign-off ready flows, jointly developed with the leading EDA providers, offer robust support for implementing designs using sophisticated multi-die packaging techniques, leveraging through-silicon vias (TSVs) in 2.5D silicon interposers and new bonding approaches.

Multi-vendor support is available, with full implementation flows from Synopsys and Cadence Design Systems. Physical verification with Mentor Graphics' suite of tools is included in the flow.

The GF 2.5D technology addresses the challenges of multi-die integration with solutions for front-end steps such as via-middle TSV creation, and flexibility for the backend steps, like bonding/debonding, grinding, assembly, and metrology.

"Our 2.5D technology provides designers with a path to enable heterogeneous logic and logic/memory integration, offering increased performance and reduced power consumption, without the need for additional packages," said Andy Brotman, vice president of design infrastructure at GF. "These benefits can now be realized very efficiently with certified design flows that provide support for the additional steps and design rules involved in the design process. By working closely with our EDA partners, we can greatly reduce the development time and time-to-production using the most advanced multi-die approaches."

The flows allow designer to quickly and reliably address the additional requirements of 2.5D design, including top-level interposer design creation and floor planning, as well as the increased complexity of using TSVs, front-side and back-side bumps, and redistribution layer (RDL) routing. The flows support the need for additional verification steps brought on by 2.5D design rules.

The design flows work with GF's process design kits (PDKs) to provide real examples that demonstrate the entire flow. The user can download the design database, the PDK, detailed documentation and multi-vendor scripts to learn how to set up and use the GF design flow. The flows use open source examples and provide the customer with working, executable and customizable flows.

The flows come with a CPU core and memory IP and all the scripts and settings to execute a Synopsys Galaxy™ Implementation Platform-based flow or Cadence Encounter®-based implementation flows with the GF PDK. Similarly, the Mentor Calibre® 3DSTACK tool is exercised in the flow to verify DRC, LVS and extraction within and between the various die stacks leveraging the same golden design kits as used inside of GF.

Comprehensive design support

The flows provide support for a complete 2.5D design flow. This includes RDL routing between chips on interposer and RDL routing to IO pads. The flows demonstrate all the steps involved in chip pad setup, C4 and microbump placement, and TSV alignment. Designers can use the flows to be guided through processes such as creating top die (logic and memory) with microbumps, followed by interposer creation – including floor planning, microbump, TSV and C4 Bump placement, power mesh generation and signal routing.

The flow incorporates the Cadence 3D-IC solution, which supports all three driving design methodologies: package driven, SoC driven, and custom driven. The solution has been proven on a number of designs ranging from 2.5D to full 3D. All of the requisite technology features are supported and accessible across environments to help unify the design, analysis and signoff tasks on the multiple die and substrate. The Cadence 3D-IC solution includes the Encounter Digital Implementation System with a 3D option.

The Synopsys Galaxy Implementation Platform has been enhanced specifically to address 2.5D design. Designers can implement the Synopsys IC Compiler™ tool for placement, assignment and routing of microbump, TSV, probe-pad and C4; microbump alignment checks; RDL and signal routing, and power mesh creation on silicon interposer interconnection layers. Advanced verification and analysis support is also available for layout vs. schematic (LVS) connectivity and design rule checking (DRC) between stacked die; parasitic extraction for TSV, microbump, RDL; signal routing metal for stacked die and silicon interposer design interconnection; and timing analysis of multi-die systems.

The flows allow for interposer and top-die physical/logical interface and alignment checks at various stages in the design phase. Mentor's Calibre can be used to verify physical offset, rotation, and scaling at die interfaces. The Calibre 3DSTACK product also enables connectivity tracing and extraction of interface parasitic elements needed for multi-die performance simulation.

- Galaxy Implementation Platform

About GF

GF is the world's first full-service semiconductor foundry with a truly global footprint. Launched in March 2009, the company has quickly achieved scale as the second largest foundry in the world, providing a unique combination of advanced technology and manufacturing to more than 160 customers. With operations in Singapore, Germany and the United States, GF is the only foundry that offers the flexibility and security of manufacturing centers spanning three continents. The company's three 300mm fabs and five 200mm fabs provide the full range of process technologies from mainstream to the leading edge. This global manufacturing footprint is supported by major facilities for research, development and design enablement located near hubs of semiconductor activity in the United States, Europe and Asia. GF is owned by the Advanced Technology Investment Company (ATIC). For more information, visit http://www.globalfoundries.com.